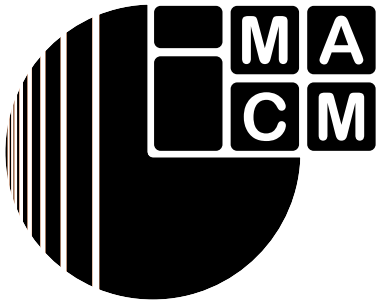

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***Abstract*—The FP7 project nanoCOPS derives new methods for simulation during development of designs of integrated products. It covers advanced simulation techniques for electromagnetics with feedback couplings to electronic circuits, heat and stress.**

I. Introduction

Designs in nanoelectronics often lead to large-size simulation problems and include strong feedback couplings. Industry demands the provisions of variability to guarantee quality and yield. It also requires the incorporation of higher abstraction levels to allow for system simulation in order to shorten the design cycles, while at the same time preserving accuracy. The nanoCOPS FP7 project addresses the simulation of two technically and commercially important problem classes identified by our industrial partners (NXP Semiconductors, ON Semiconductor, ACCO Semiconductor, and MAGWEL) [8]:

- **Power-MOS devices**, with applications in energy harvesting, that involve couplings between electromagnetics (EM), heat and stress, and
- **RF-circuitry** in wireless communication, which involves EM-circuit-heat coupling and multirate behaviour, together with analogue-digital signals.

To meet market demands, the **scientific challenges** are to:

- create efficient and robust simulation techniques for strongly coupled systems, that exploit the different dynamics of sub-systems and that allow designers to predict reliability and ageing;
- include a variability capability such that robust design and optimization, worst case analysis, and yield estimation with tiny failure probabilities are possible (including large deviations like 6-sigma);
- reduce the complexity of the sub-systems while ensuring

that the operational and coupling parameters can still be varied and that the reduced models offer higher abstraction models that are efficient to simulate.

Achieving solutions to these challenges will have considerable **industrial impact**. The overall **objective** of nanoCOPS is to advance a methodology for circuit-and-system-level modelling and simulation based on best practice rules to deal with **coupled electromagnetic field-circuit-heat problems** as well as **coupled electro-thermal-stress problems that emerge in nanoelectronic designs**. The new methods developed are robust and allow for **strong feedback coupling** when integrating systems to increase the performance of both existing devices and when integrating systems to produce new devices.

With the new techniques it is possible to efficiently analyze the effects due to **variability**. Our methods are designed to solve **reliability** questions arising from **manufacturability**. They facilitate robust design as well as enable worst case analysis. They can also be used to study effects due to ageing. **Ageing** causes variations in parameters over a long-term period, which cannot be predicted exactly and thus are typically uncertain. The challenges for an Integrated Circuit (IC) are that each device has its own electrical and thermal conditions, which are changing over time (due to ageing, for example). Here, each device has its own required life-time.

Novel **Model Order Reduction** techniques, developed here for the fast repeated simulation of the coupled problems under consideration, are applicable to both coupled systems and parameterized sub-systems. As such they are an essential ingredient for the Uncertainty Quantification.

In summary, our **solutions** are

- advanced co-simulation/multirate/monolithic techniques, combined with envelope/wavelet approaches;
- new generalized techniques in Uncertainty Quantification (UQ) for coupled problems, tuned to the statistical demands from manufacturability;

TABLE I
PARTNERS IN NANOCOPS

Abbr.	Partner
BUW	Bergische Universität Wuppertal, Germany (coordinator)
HUB	Humboldt Unversität zu Berlin, Germany
TUD	Technische Universität Darmstadt, Germany
UGW	Ernst-Moritz-Arndt-Universität Greifswald, Germany
FHO	FH OÖ Forschungs- und Entwicklungs GmbH, Hagenberg im Mühlkreis, Upper Austria, Austria
KUL	Katholieke Universiteit Leuven, Belgium
BUT	Vysoké učení technické v Brně, Brno University of Technology, Czech Republic
MPG	Max Planck Institute for Dynamics of Complex Technical Systems, Magdeburg, Germany
NXP	NXP Semiconductors Netherland B.V., Eindhoven, The Netherlands
ONN	ON Semiconductor Belgium, Oudenaarde, Belgium
MAG	MAGWEL NV, Leuven, Belgium
ACC	ACCO Semiconductor, Louveciennes, France

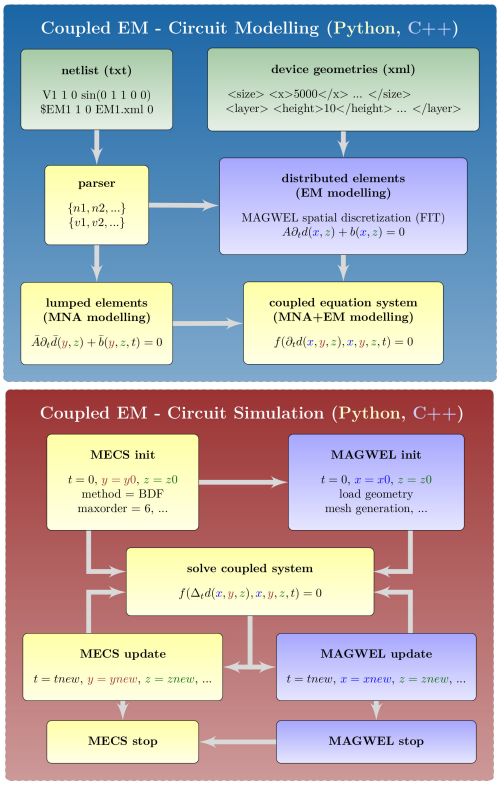


Fig. 1. Set up for coupled modelling (top) and simulation (bottom).

- enhanced, parametric Model Order Reduction techniques for coupled problems and for UQ.

All the new algorithms produced are **implemented and transferred** to the SME partner MAGWEL. **Validation** is conducted on industrial designs provided by our industrial partners. These industrial end-users provide feedback during the project life-time and contribute to measurements and provide material data and process data. A thorough comparison to **measurements** on real devices is being made to demonstrate the industrial applicability.

Our consortium brings together extensive R&D experience in nanoelectronic IC simulation and complementary areas of expertise. It includes seven universities, one research institute, two large-scale semiconductor companies, and two SMEs, see Table I.

II. Progress and Results

Below we give an impression of outcomes achieved in the first half of the project duration. We refer with the abbreviations in Table I to the various project partners.

A main result, through joint effort by **MAG, HUB, FHO, TUD**, was the development of a simulation environment, which both enables the co-simulation [7], [9] and monolithic/holistic simulation of a circuit/device system or electrical-thermal systems, see Fig. 1. The interface,

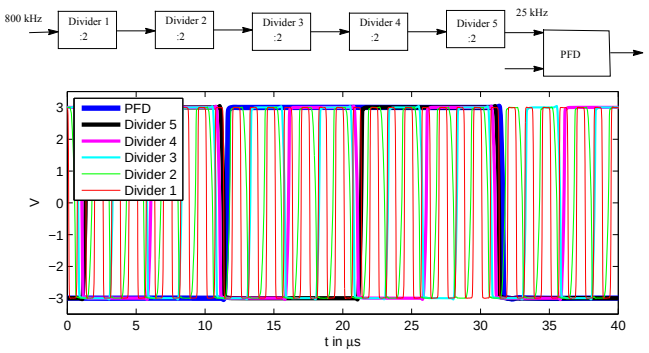


Fig. 2. Divider block diagram and multirate solution, which was efficiently solved by the implementation of FHO.

both linear and nonlinear, couples software modules from academia to the device and electromagnetic field simulator from MAGWEL, offering flexibility in adapting modules and allowing for different time integration procedures. In this way, coupling of electronic circuits with electromagnetics and with semiconductor material is achieved. It also allows for state-space formulations of subparts to which Model Order Reduction can be applied. The interface keeps the space discretization in the field simulator and generates a system of Differential-Algebraic Equations (DAEs). Especially, when including semiconductor material, large differences of magnitude made careful scaling during the assembly essential to guarantee that the overall system was stable [2], [13].

FHO developed a multirate envelope time-integration technique, which combines decompositions along two time scales [4]. Emphasis is on performance optimization, including adaptive grids, iterative linear solvers for huge problems (e.g. preconditioned GMRES), optimization of the evaluation of lumped devices (e.g. BSIM3 and BSIM4, MEXTRAM, etc.). Fig. 2 shows the divider block diagram for a PLL in the 5.6 GHz ISM band, employing the silicon germanium technology of IHP (a research center funded by the German government). The simulation of frequency dividers is a severe bottleneck for PLL simulation and for the multirate technique in general. Adaptive methods are employed for the different stages of the divider. Table II shows the dramatic improvement of the run time using adaptivity. No commercial circuit simulator provides this facility yet.

UGW, BUW, MAG, TUD worked on methods for Uncertainty Quantification and applied the approaches to address variations of material properties as well as in the geometry [11]. Apart from in-house software from UGW and BUW, interfacing with libraries from Sandia National Laboratories [5] was achieved. In order to demonstrate robustness, a Power Transistor Model was optimized. We reduced the thermal instability by optimizing the geometry within the device layout, while taking both the conductive power losses and the

TABLE II
PERFORMANCE SUMMARY MULTIRATE SIMULATION.

	Single Grid	Multiple Grids
Number of equations	130,000	85,000
Nonzeros in Jacobian	5×10^6	2.5×10^6
Assembly of Linear System	4s	2s
Linear Solve	8s	4s
Envelope Analysis	5h	37min

robustness into account. The Stochastic Collocation Method provided a response surface model that could be used for robust topology optimization. Combining with a Topological Derivative Method, we could reduce hot spot phenomena in a robust sense, see Fig. 3. Our implementations are also able to identify dominant parameter contributions to mean and standard variation when varying parameters.
TUD developed a GUI (Graphical User Interface) for Uncertainty Quantification to easily compare our UQ methods with Monte Carlo simulations and Worst Case Corner Analysis. The last approach is very popular in the semiconductor industry because it is much faster than Monte Carlo and thus offers an excellent challenge for demonstrating benefits with UQ. Our UQ implementation exploits sparse grid techiques and can easily deal with up to 20 independent parameters.

Bondwires, see Fig. 4, are the most common way to establish electric connections between the chip and the lead frame or pins during fabrication. **TUD** and **ONN** have focused an improved electrothermal formula that is the basis for a bondwire calculator for ONN [6]. Bondwire temperature can

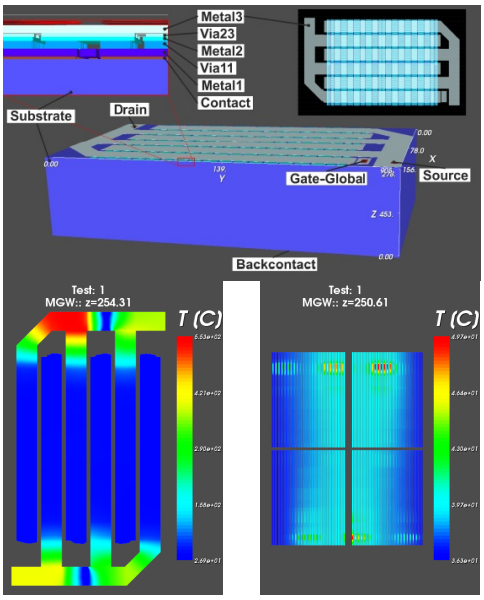


Fig. 3. Power Transistor (top) optimized to reduce power hotspots while taking geometrical variations into account. The pictures at the bottom give a temperature distribution in the Metal3 layer and the Contact Layer for the structure after optimization (joint work by UGW, BUW, MAG).

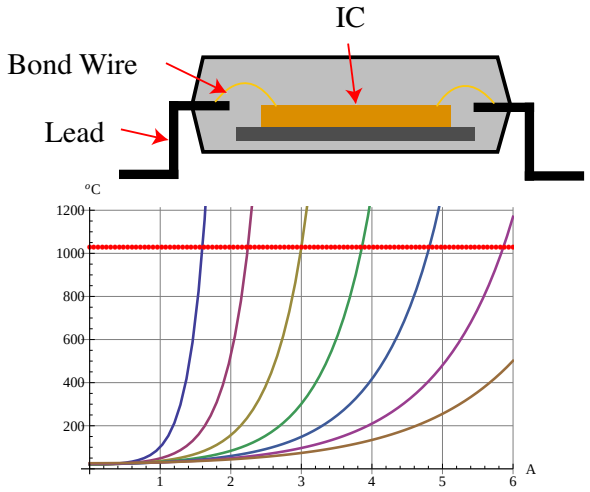


Fig. 4. Top: Classic IC lead-frame package. Bottom: Au-wire current capacities for several diameters and a fixed length. The plotted temperature is at the wire mid-point, where the hottest point is expected.

increase substantially since the electric power is supplied through the wires. If the wires cannot properly dissipate this energy, then permanent damage will occur to the wires and surrounding material. A mathematical formula has been developed that improves the prediction of this heating compared to known models from literature. The formula retains important geometrical parameters defining the package, which adds high flexibility. This reduces the over-design of the wires during fabrication. The evaluation of this formula is computationally inexpensive such that time-consuming 3D simulation can be avoided. However, a coupling of the bondwire model to a 3D simulator is necessary if the integration in the overall system behaviour should be simulated. Thus, TUD also implemented a nonlinear in-house simulation code based on the Finite Integration Technique (FIT) to analyze the coupling before transferring the concept to partner MAG. ONN aims to use the algorithm within a GUI.

ONN and **BUT** made measurements of DC and dynamical fusing of bondwires [10]. ONN fabricated test chips (SOIC package so far), where the individual bondwires with different lengths, diameters and materials have been encapsulated. BUT prepared a complete methodology and experimental setup to do such investigations.

The setup (hardware tester and MATLAB GUI) allows measurements of all six bondwires in one IC package. The tester consists of the 6 independent channels, the 6 driving stages, the 6 Kelvin probe sensing stages, the demultiplexing core for the driving stages (specification of address of the bondwire) and the multiplexing core for the Kelvin probe sensing stages.

The block structure, the single channel operation and photographs of the final hardware solution are shown in Fig. 5. The frequency limitation of the measurement setup is about 500 kHz (limits of used MOS power-switches and

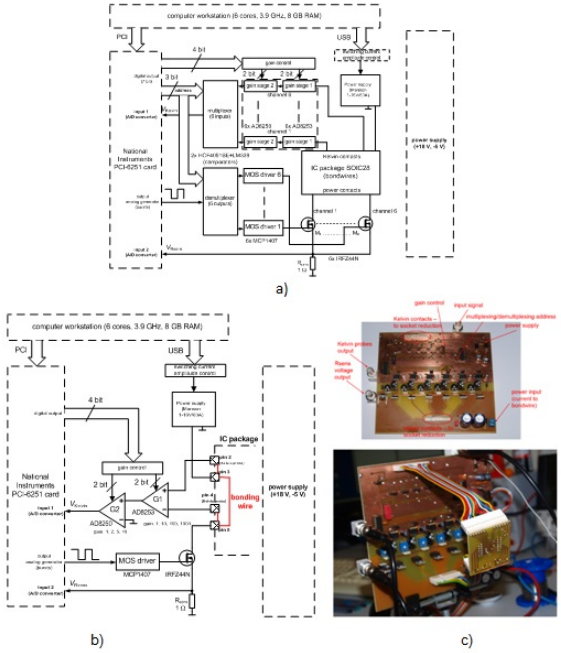


Fig. 5. Final hardware solution of the bondwire tester prototype: a) overall block structure, b) single channel principle, c) final version of the PCB.

PCI card). The software part of the project consists of two executable MATLAB scripts with a GUI. MATLAB software is also used for the generation of testing sequences and signals that drive the tester. Finally, the measurements have been used to validate the bondwire formula.

MAG and **ONN** co-operated on electro-thermal simulation in order to guarantee industrial acceptance. An important highlight of this work is that the electro-thermal simulation tool is very flexible concerning the various device technologies since the nanoscale transistor architecture is incorporated via compact models. Therefore, it is possible to couple the large-scale (millimeter) structures and the small-scale (sub-micron) of the finger architecture in a single simulation. The computation deals with the coupling of the electrical response and with the thermal response in first-principle field solving. Fig. 6 illustrates today's capabilities [12].

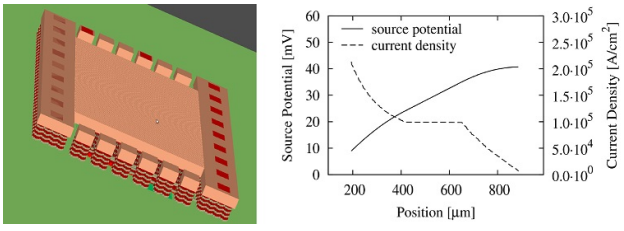


Fig. 6. Analysis of a power MOS (left figure) resulting into an asymmetric current density due to thermally induced conductance variations in the metallic interconnect (right figure).

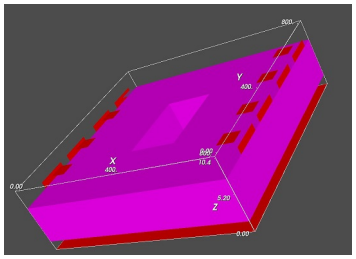


Fig. 7. A package model (provided by MAG).

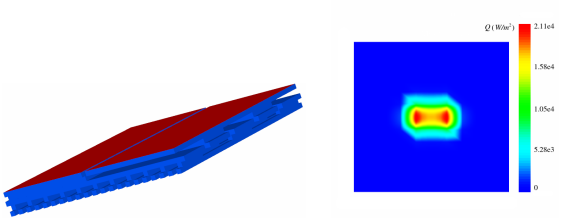


Fig. 9. Left: Power-MOS device (the back contact is not shown). Right: Heat flux density on the back contact at time $t = 10^{-6}$ s.

MPG and **MAG** developed efficient parameterized Model Order Reduction (pMOR) methods and techniques for fast simulation of electro-thermal coupled models [1], [3] and for fast Uncertainty Quantification [15] of nanoelectronic, electro-thermal models with random variables or stochastic processes. Linear parametric models in state-space-form were constructed based on the discrete data provided by MAG. As an example we consider a parametric thermal package model, see Fig. 7. Accurate reduced-order models were derived for these linear parametric models. Structure preserving models with sufficient accuracy are obtained for nonlinear parametric coupled problems as well. See Fig. 8 for the results of the reduced-order model. The relative error of the output produced by the reduced-order model (ROM) is of the order 10^{-11}. In developing pMOR methods for fast UQ of nanoelectronic, electro-thermal models with random variables or stochastic processes, we applied pMOR techniques to a Power-MOS device (Fig. 9), provided by MAG, and obtained a parametric reduced model (pROM) that is of high accuracy over a very large parameter range. We have embedded the parametric reduced model into the Stochastic Collocation Method, which proved to be both efficient and accurate.

Fig. 9 shows the heating of the chip. We built an order-2 pROM for the order-1660 Full Order Model (FOM) of the electrical part, and an order-50 pROM for the order-11556 FOM of the thermal part. Fig. 10 depicts the evolution of the "maximal relative error at the outputs", which is defined as the maximal relative error at all outputs. When the system starts, the maximal relative error is high because the system is hardly heated up (exact values close to 0) and the thermal parts are dominated by modelling error and numerical error. However, as time elapses, the maximal relative error goes down to the order of 10^{-4} and therefore, the dominant physical properties are accurately captured over a large parameter range.

NXP, **BUW** and TU Eindhoven developed a special algorithm for fast fault simulation in NXP's in-house circuit simulator Pstar - when considering this from the point of view of parameter variations this is well in the range of large deviations. NXP's simulator is the best in the world in this area [14]. They can identify locations on a chip that are probably affected by very tiny manufacturing inaccuracies and thus causing faulty behaviour at predefined time points for measurements. Each candidate fault is a low-rank modification of the designed circuit. Inclusion of sensitivity analysis brought speeds up in CPU time of a factor 20 or more. See Fig. 11 for an indicative result. Later invoking of faults gave an additional order of magnitude in speed up. By this reduction of simulation time candidate faults could be detected that would have been impossible otherwise because of excessive CPU time.
This algorithm offers interesting ingredients to combine with Uncertainty Quantification.

ACC has prepared several designs, made simulations and realized test boards. They will be used for step by step study, measurements and validation of the enhanced MAGWEL software, in close cooperation with **BUT**, **NXP** and **ONN**. The bigger designs can also be used for final validation in

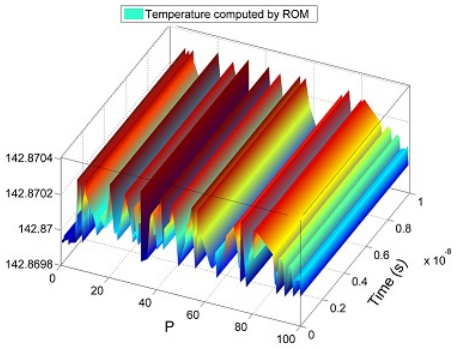
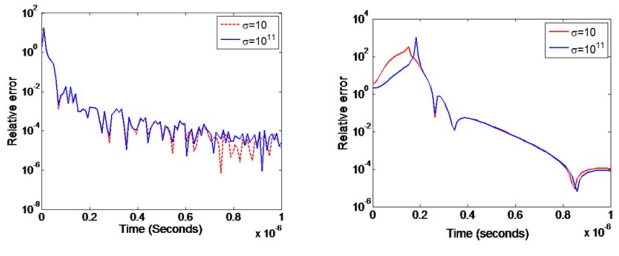


Fig. 8. Full order model state space $n = 8549$, ROM state space $r = 58$, amount of inputs 34 and outputs 68. Temperature as computed by the ROM.



(a) Rel. Error at Source (b) Rel. Error at Back Contact

Fig. 10. The evolution of the maximal relative error of the outputs for different values of the electrical conductivity $\sigma = 10,\ 10^{11}$ S/cm.

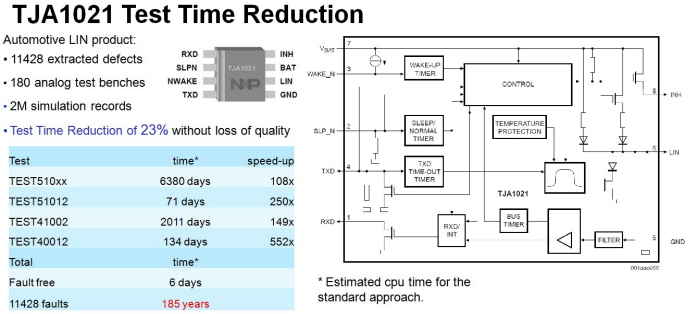


Fig. 11. Speed up in fast fault simulation for the TJA1021 chip.

adddition to the industrial use cases.

As simple example, we mention here test chips that include passive structures (inductances, capacitances, baluns, resonators). These structures, that are easily measurable, will be used to validate EM extraction and model reduction. Simulated results will be compared to measurements, EM solver extraction and then with extraction plus netlist reduction in terms of accuracy, memory usage and time simulation.

III. Conclusion

The unique combination of the nanoCOPS consortium allows to already report the following intermediate, innovative highlights halfway the project, to which all partners have contributed.

- The coupling interface with the MAGWEL software has been improved, tested and is operational.
- Successful large-scale EM-heat simulation was achieved.
- Grid-adaptive multirate circuit simulation was established.
- Model Order Reduction was successfully applied to coupled EM-Heat problems.
- Accurate bond wire modelling for fast usage at industry was demonstrated and was validated by measurements.
- Uncertainty Quantification was applied to variations of material parameters and geometry and was used in robust topology optimization. Apart from the topics, this at best demonstrates the robustness of the integrated software - to achieve optimization one addresses all parts of the codes.
- Innovative methods for improving yield as well as to identify faults were derived.
- Advanced measurements environments have been set up both at academia and at industry.
- Outcomes have been presented at conferences. Joint papers have been published in various journals.
- Interaction between academia and industrial partners addressed a broad range: test examples, new algorithms, implementations, practical use of new methods, ways to improve measurements.

Acknowledgment

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