Bergische Universität Wuppertal

Fachbereich Mathematik und Naturwissenschaften

Lehrstuhl für Angewandte Mathematik
und Numerische Mathematik

Preprint BUW-AMNA 04/08

Andreas Bartel, Uwe Feldmann

Modeling and Simulation for Thermal-Electric Coupling in an SOI-Circuit

September 2004

http://www.math.uni-wuppertal.de/org/Num/

Modeling and Simulation for Thermal-Electric Coupling in an SOI-Circuit

Andreas Bartel[1] and Uwe Feldmann[2]

[1] Lehrstuhl für Angewandte Mathematik/Numerische Analysis, Universität Wuppertal, D-42097 Wuppertal, Germany, bartel@math.uni-wuppertal.de
[2] Infineon Technologies AG, Balanstr. 73, D-81541 München, Germany, Uwe.Feldmann@infineon.com

Summary. In Silicon on Insulator (SOI) circuits thermal effects are of particular relevance due to restricted cooling via the substrate. The accompanied thermal network enables to include one dimensional heat conduction effects to the lumped electric network equations. In this framework for thermal-electric coupling, we model an industrial-like benchmark based on a simple ring oscillator circuit. This is to picture abstractly the on-chip behavior by simple means. After a rough description of an applied simulation technique multirate results for this example are given. These underline the huge saving potential according to the widely separated timescales of electric networks and heat conduction.

Key words: Electric circuit simulation, heat conduction, temperature dependence, parabolic partial differential algebraic equations.

1 Introduction

Due to miniaturization of devices and the increasing package densities, the dissipated power per chip area increases. Since semiconducting devices and interconnects in chip technology are temperature sensitive and even may be destroyed in hot spots, it is important to include the heat evolution into circuit analysis. Usually, this is done by thermal networks, which include the local temperature and its cooling towards environment. Since this cooling is limited especially in SOI (Silicon on Insulator) technologies, the heat conduction phenomenon becomes more pronounced. And this is aggravated by decreasing spacing between devices in higher package densities.

Therefore, an approach to include one dimensional thermal effects is introduced in the next section. It is the so-called accompanying thermal network (AN), which completes the network equations. As a benchmark example we then discuss a ring oscillator circuit and its thermal description using the AN. The fourth section presents numerical results, which are computed by exploiting the multirate setting of this system. Finally we draw some conclusions.

2 Mathematical Model

To extend the more or less standard lumped thermal approach for modeling heat conduction, a spatial model needs to be provided. As a first step towards full 3D-modeling, the accompanied thermal network (AN) [BaGü03, Ba03] includes heat conduction in one spatial dimension. These can be macro-structures on chip into any preferred direction of conduction: for instance, cell arrays, interconnects, or others. Also one can picture this model as order reduced real world, where a designer has specified macro-structures. In power circuits with a relatively small number of power dissipators, such an order reduction can be performed on the set of equations, see [WCSW97].

To have both lumped and spatial 1D-thermal element models, the AN needs to couple both descriptions. The interface is established by a flux condition, which enables the use of standard schemes for setting up equations within this formulation. For the overall thermal-electric problem, we obtain the system of equations in Box 1. The concurring systems are the following: first we have the common electric network equations [Ti99] in terms of the node voltages $\mathbf{u}$ and branch currents $\boldsymbol{\jmath}_L, \boldsymbol{\jmath}_V$ (with topology $\mathbf{A}$); the second part, the AN, is basically a coupled system of energy balance equations for both types of elements; these use 1D and 0D temperatures $\mathbf{T}$ and $\widehat{\mathbf{T}}$, respectively. The temperatures enter the network equations via parameters of the

Box 1: Coupled thermal-electric problem.

electric network: (DAE-IVP) $\quad \mathbf{A} = (\mathbf{A}_C, \mathbf{A}_G, \mathbf{A}_L, \mathbf{A}_S, \mathbf{A}_I, \mathbf{A}_V)$

$$\begin{aligned}\mathbf{0} &= \mathbf{A}_C\dot{\mathbf{q}}(\mathbf{A}_C^\top\mathbf{u}(t)) + \mathbf{A}_G\mathbf{r}(\mathbf{A}_G^\top\mathbf{u}(t), \boxed{\mathbf{T}^{\mathrm{br}}, \mathbf{F}}) + \mathbf{A}_L\boldsymbol{\jmath}_L(t)\\ &\quad + \mathbf{A}_S\boldsymbol{\jmath}(\mathbf{A}_C^\top\mathbf{u}, \boxed{\mathbf{T}^{\mathrm{br}}, \mathbf{F}}) + \mathbf{A}_I\boldsymbol{\imath}(t) + \mathbf{A}_V\boldsymbol{\jmath}_V(t)\\ \mathbf{0} &= \dot{\boldsymbol{\phi}}(\boldsymbol{\jmath}_L(t)) - \mathbf{A}_L^\top\mathbf{u}(t)\\ \mathbf{0} &= \mathbf{A}_V^\top\mathbf{u}(t) - \boldsymbol{v}(t) \qquad (1a)\end{aligned}$$

(IV) $\quad \mathbf{x}(t_0) = (\mathbf{u}_0, \boldsymbol{\jmath}_{L,0}, \boldsymbol{\jmath}_{V,0})^\top \qquad (1b)$

coupling interface: $\quad (\boldsymbol{\lambda}_P = \boldsymbol{\lambda}_P(\mathbf{u}, \boldsymbol{\jmath}_L, \boldsymbol{\jmath}_V))$

$$\mathbf{P}_{\mathrm{tr}}, \mathbf{P}_{\mathrm{lp}}{}^\top = \mathbf{P} = \mathrm{diag}\ \mathbf{K}\boldsymbol{\lambda}_P\ \mathbf{A}_{\mathrm{tp}}^\top\mathbf{u}, \quad \mathbf{F} = \mathbf{F}(\mathbf{T}), \quad \mathbf{T}^{\mathrm{br}} = \mathbf{Q}^\top\widehat{\mathbf{T}} \qquad (1c)$$

thermal network: (PDAE-BIVP) $\quad i = 1, \ldots, m$

$$\text{(1D)}\quad M_i\dot{T}_i(x,t) = \partial_x\ \Lambda_i\partial_x T_i(x,t)\ - \gamma S_i\cdot(T_i(x,t) - T_{\mathrm{env}}) + \widetilde{P}_i(x,t) \qquad (1d)$$

$$\widetilde{P}_i(x,t) = \sum_{k=k_i}^{l_i} \boxed{P_{\mathrm{tr},k}(t)}\cdot\frac{\widetilde{\rho}_k(x,T_i)}{R_k(t,T_i)}, \quad R_k = \int_0^1 \widetilde{\rho}_k(x, T_i(x,.))\,\mathrm{d}x \qquad (1e)$$

$$\text{(0D)}\quad \widehat{\mathbf{M}}\dot{\widehat{\mathbf{T}}}(t) = \mathbf{A}_{\mathrm{AN}}\ \begin{matrix}\boldsymbol{\Lambda}(0)\partial_x\mathbf{T}(0,t)\\ -\boldsymbol{\Lambda}(1)\partial_x\mathbf{T}(1,t)\end{matrix}\ -\gamma\widehat{\mathbf{S}}(\widehat{\mathbf{T}} - T_{\mathrm{env}}\mathbb{1}_k) + \mathbf{Q}\boxed{\mathbf{P}_{\mathrm{lp}}(t)} \qquad (1f)$$

$$\text{(BC)}\quad \begin{matrix}\mathbf{T}(0,t)\\ \mathbf{T}(1,t)\end{matrix} = \mathbf{A}_{\mathrm{AN}}^\top\widehat{\mathbf{T}}(t) \qquad (1g)$$

$$\text{(IC)}\quad \mathbf{T}(x,0) = \mathbf{T}_0(x) \geq T_{\mathrm{env}}\mathbb{1}_m \qquad \widehat{\mathbf{T}}(0) = \widehat{\mathbf{T}}_0 \geq T_{\mathrm{env}}\mathbb{1}_m \qquad (1h)$$

static part (using branch temperatures $\mathbf{T}^{\mathrm{br}}$ and functionals $\mathbf{F}$ – $\mathbf{Q}$ identifies the according thermal 0D-unit for the thermally lumped electric elements); vice versa, the dissipated powers P of passive electric elements ($\mathbf{A}_{\mathrm{tp}}$) yield source terms for the AN. – The existence of solutions of this system and its well-posedness will be the topic of [BaGJ04].

3 AN for SOI Circuits

In the following, we construct a benchmark to reflect the complex on-chip behavior of SOI circuits in a simplified way. One main component is a standard ring oscillator, which is composed CMOS-inverters in SOI technology as depicted in Fig. 1. In the left-hand part, several inverters are connected in

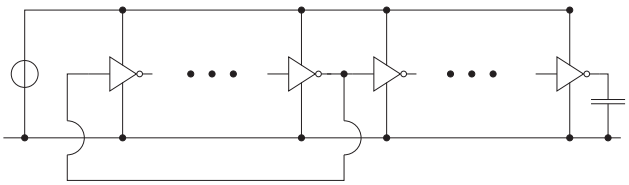

Fig. 1. Industrial benchmark – electric network.

feed back configuration to form an autonomous oscillator. This unit drives a cascade of inverter stages in the right-hand part. In total, this configuration may model an inner chip signal-flow (e.g. a critical path): part one provides the logic or analog functionality, while part two serves for signal amplification or for driving output signals. For simplicity, the involved CMOS-inverters are here described using the standard level-1 transistor model of Shichman-Hodges [ShHo68]. Consequently, the benchmark circuit in Fig. 1 represents a network of basic elements, where semiconducting devices are replaced by capacitances, diodes and controlled current sources.

Here the major temperature T dependence is given by the mobility of charge carriers. It enters the system by the scaling factor β of the controlled current source modeling the transistor channel between drain and source

$$\imath_{ds}(u_{gate}, u_{source}, u_{drain}, u_{bulk}, T) = \beta(T) \cdot \widehat{\imath}_{ds}(u_{gate}, u_{source}, u_{drain}, u_{bulk}),$$

(with $u_{gate}, u_{source}, u_{drain}, u_{bulk}$: potential of gate, source, drain, bulk node)

$$\beta = \mu(T) \cdot C'_{ox} W/L,$$

where mobility μ strongly depends on device temperature T; W and L refer to the transistor's width and length, and capacitance C'_{ox} is the capacitance per unit area for the oxide layer between gate and channel (see Box 2). Now, mobility decreases with temperature nonlinearly, which can be approximated as [MaAn93]

$$\mu(T) = \mu(300\,\mathrm{K})\left(\tfrac{T}{300\,\mathrm{K}}\right)^{-1.5}.$$

In this example, the concurring p- and n-type devices (in CMOS technology) are electrically separated in one-dimensional arrays. Since the thermal and electric insulation comes along with each other, we have in first order only a thermal link for transistors of the same type. Heat transfer to the bottom of the chip is small here due to high thermal resistance of the insulating oxide layer in SOI technology. Therefore the AN for this example consists of two decoupled 1D-lines following the arrays of n- and p-type transistors. The situation is sketched in Fig. 2; the dotted lines signify the electrical connection

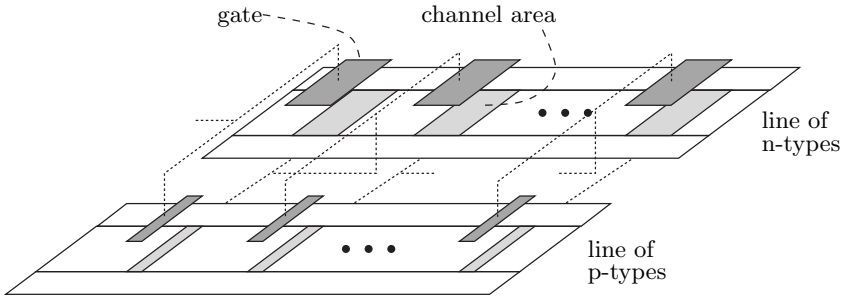

Fig. 2. Thermal 1D-lines.

to recognize the layout of this benchmark circuit. The devices' main currents pass just below the gates, through the channel area. There the main power is dissipated. Since the driver-units are scaled to amplify electric signals, we expect a large heat production there. This will further heat the remaining circuit, and cause a signal delay in the oscillatory part.

For simplicity, we consider a reasonably sized test circuit with only three inverter stages in the oscillator and a cascade of five bootstrap inverters. The latter are scaled to drive the load capacitance (see Fig. 1). The scaling is applied to the width for both n- and p-type transistors and takes the following values from left-to-right: 1, 2, 5, 10, 25.

To form a thermal-electric coupling the geometric data of the 1D-line are necessary. Here we assume that successive devices are spaced by a distance of $4\,W_n (= 2\mu\mathrm{m})$, where W_n is the width of n-channel device in the oscillator (see Box 2). Oscillator and driver unit are separated by an additional spacing of distance $8\,W_n$.

In this setup, the driver stages exhibit a thermal 1D-extension, which excites the ring oscillator stages. Therefore the formation of a special 0D-unit is inappropriate and we embed the driver stages to the 1D-lines. Consequently, the two 1D-lines in the AN have attached artificial 0D-units [Ba03], which form a zero flux condition (von-Neumann BC).

For the electric-to-thermal coupling, we equally distribute the (lumped) dissipated power on the respective transistor's location (width): for type $i \in \{\mathrm{n}, \mathrm{p}\}$ and the kth device in line, we have

Box 2: Typical Parameter for Shichman-Hodges.

Geometric parameters:		
width:	$W_n = 0.5\,\mu$m	$W_p = 1.5\,\mu$m
length:	$L = 0.2\,\mu$m	
thickness channel-gate oxide:	$t_{ox} = 3.0\,$nm	
thickness buried oxide:	$t_{box} = 34.5\,$nm	
Model parameters:		
mobility:	$\mu_n(300) = 400\,\mathrm{cm}^2/(\mathrm{Vs})$	$\mu_p(300) = 130\,\mathrm{cm}^2/(\mathrm{Vs})$
thres. voltage (enhanced):	$V_{th}^n = +250\,$mV	$V_{th}^p = -250\,$mV
overlap capacitance per width:	$C'_{ov} = 0.4\,$nF/m	
junction capacitance per width:	$C'_j = 2.0\,$nF/m	
saturation current:	$I_S = 1.0 \cdot 10^{-15}$A	

$$P_{i,k} = \imath_{ds}^{i,k} \cdot u_{ds}^{i,k}$$

with the corresponding 1D-indicator function $\widetilde{\rho} = \chi_{i,k}$ (this simply locates the device in 1D-line segment). In this way, we obtain the continuous thermal model, equation (1d), where the local power source term is given as

$$\widetilde{P}_i(x,t) = \sum_{k=1}^{s} P_{i,k}(t) \cdot \frac{\chi_{i,k}(x)}{R_{i,k}}, \qquad R_{i,k}(= W_{i,k}) = \int_0^1 \chi_{i,k}(x)\,\mathrm{d}x$$

for the two lines ($i \in \{\mathrm{n}, \mathrm{p}\}$) and a total number of $s = 8$ inverter stages. In turn, the lumped temperatures can be obtained by averaging the temperature with the indicator function as weight (thermal-to-electric coupling). Thus mobilities are obtained by evaluation at the derived temperature.

The second source term in (1d) is cooling. It is proportional to the local surface (perimeter) S. Here several sides of the 1D-line are covered by oxide limiting the heat flow to environment. But there are additional electric contacts at the devices. These metal interfaces can be treated as additional surfaces whose transmission coefficient γ is several orders of magnitude larger.

The next step is discretization. A simple and applied choice are finite volumes; these fit to the AN-setting: each device and each interspacing gets an own cell, cf. Fig. 2, giving a rough scale of thermal resolution. Here the device's total length is condensed to a point in the 1D-line, the width is represented by the according line segment. Parameters for this benchmark circuit are summarized in Box 3.

Box 3: Thermal Ring oscillator.

Geometry	1D-quantities
load capacitance: $C_L = 200\,$pF	heat mass (Si): $M = 3.5\,10^{-8}\,$J/m K
surface: $\gamma S = 2.4\,\mu$W/mK $(+4.8\,10^{-2})$	conductivity: $\Lambda = 3.18\,10^{-12}\,$Wm/K

4 Simulation Results

To enable a simple inclusion and coupling to a circuit simulator, we consider for the semi-discretized system a co-simulation approach. The spatially discrete system does not suffer from contraction conditions [ArGü00] due to DAE effects [Ba03], and enables a multirate procedure, where iteration is not necessary. To this end, an energy coupling is formed [DeTü99, Ba03]: additionally the dissipated powers are integrated together with the network equations

$$\dot{E} = \imath_{ds} \cdot u_{ds}, \quad E(0) = 0$$

over a communication step H ($[0, H]$, for simplicity). Here temperature is kept fix (or can be extrapolated). In a second step, this energy is transmitted to the AN and is equally distributed in time during the computation of the temperature. Due to on-chip dimensions, capacitances in the network equations are tiny and yield small time constants. Thus the network-power equations form a multiscaled subsystem, and rescaling is necessary.

Next, we discuss simulation. The ring oscillator begins its autonomous oscillation fast (its shape depends on the parameters). With varying temperature, signals will traverse the circuit with different speed due to the temperature dependence of mobility. – This can be seen in the output signals in Fig. 4: a lower temperature at an early time and a higher temperature at a later time. Clearly, the two signals diverge.

For MATLAB simulations, we scaled both thermal mass (M) and heat conduction (Λ) by a factor of $1/50$ and 10, respectively. This enlarges the thermal electric coupling and gives a harder numerical problem to solve, but we needed smaller simulation times to recognize thermal effects. Here the time window [0s, 50ns] is considered. For the time-integration, MATLAB routine `ode15s` was employed. Now, Fig. 3 depicts the overall temperature evolution and a startup-phase. Furthermore, Fig. 4 gives the output signal at the first inverter, showing the temperature dependence of the electric signal. Inclusion

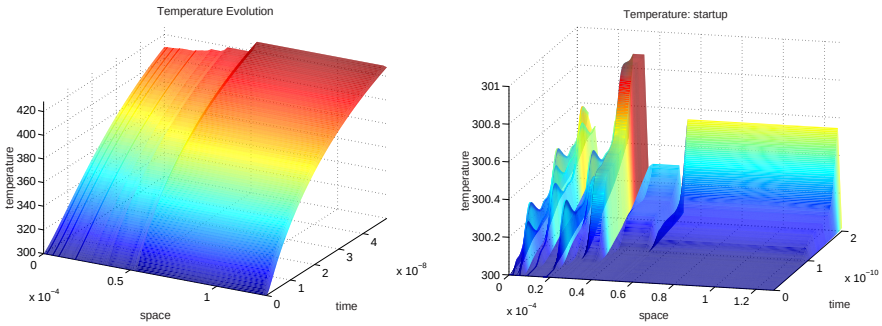

Fig. 3. Temperature distribution $[0.\,\mathrm{s}, 50.\mathrm{ns}]$ (left), startup $[0.\,\mathrm{s}, 0.2\mathrm{ns}]$ (right).

of temperature effects is indeed necessary in simulation, since their impact on signal delays is significant and may even cause malfunctions of the chip.

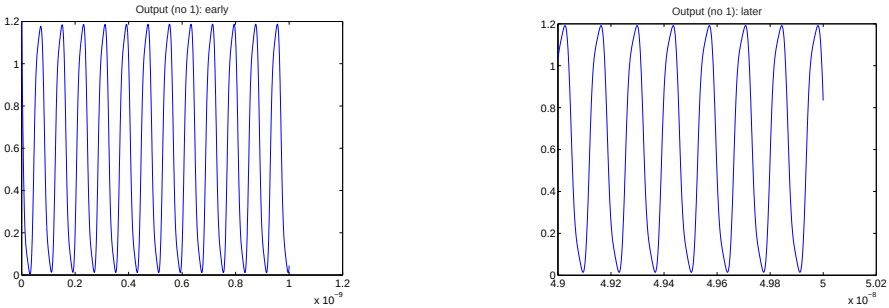

Fig. 4. Output inverter (no. 1): [0.s, 1.ns] (left), [49.ns, 50.ns] (right).

In Fig. 3 (right), we see the development of the temperature in our benchmark at a very early time. We can precisely identify the devices in our line, and we recognize the scaling and spacing of the devices. Actually, the larger p-channel devices are depicted, here.

Next, we can compare these singlerate computation (all-at-once) with results from the multirate co-simulation. Here we have chosen a communication step of 0.2 ns. At the final time, we obtain a very good agreement of both temperatures, see Fig. 5 – the error is less then 0.16 K. Since model evaluation is the most costly part in circuit simulation, we contrast the number of time

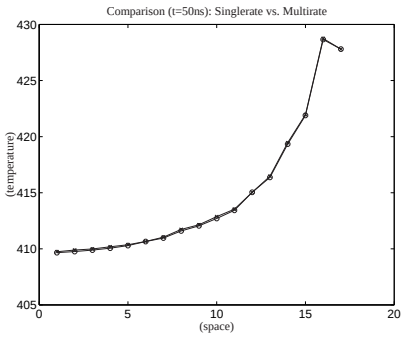

Fig. 5. Comparison: Singlerate 'o' vs. Multirate 'x'.

steps for both algorithms in Tab. 1. Indeed multirating is achieved. Notice, per communication step there is only about one step of the AN solver necessary; actually, the remaining four steps are all spent in the startup phase. Therefore due to averaging an order two method based on the mid-point rule can be constructed [Ba03]. However, recall that this multirating has its price. Additionally to the electric network, the energy equations have to be integrated. Fortunately, there was no iteration necessary for getting these accurate results.

Table 1. Results: Singlerate vs. Multirate

		steps	comm.-steps
single-rate	(total)	70 924	–
multi-rate	(network)	71 630	125
co-simulation	(heat)	129	

5 Conclusions

We have addressed the multirate behavior of the thermal-electric problem in our benchmark circuit. Since the discretized coupled system with energy coupling does not suffer from additional contractivity conditions in co-simulation, an adapted multirate strategy is applicable. Numerical tests for this benchmark example verify that indeed multirate is achieved.

Acknowledgement. This work is part of the project "Numerische Simulation von elektrischen Netzwerken mit Wärmeleitungseffekten" (03GUM3W1) supported by the German Federal Ministry of Education and Research.

References

[ArGü00] Arnold, M., Günther, M.: Preconditioned dynamic iteration for coupled differential algebraic systems. BIT, **41**:1, 1–25 (2000).

[Ba03] Bartel, A.: Partial Differential-Algebraic Models in Chip Design — Thermal and Semiconductor Problems. PhD Thesis, Technische Universität München (2003).

[BaGü03] Bartel, A., Günther, M.: From SOI to abstract electric-thermal-1D multiscale modeling for first order thermal effects. Math. Comput. Modell. Dynam. Syst., **9**:1, 25–44 (2003).

[BaGJ04] Bartel, A., Günther, M., Jüngel, A.: Existence analysis for a thermal-electric problem. In preparation.

[DeTü99] Deml, Ch., Türkes, P.: Fast Simulation Technique for Power Electronic Circuits with Widely Different Time Constants. IEEE Transactions on Industry Applications **35**:3, 657–662 (1999).

[MaAn93] Massobrio, G., Antognetti, P.: Semiconductor Device Modeling with SPICE, 2nd ed., McGraw-Hill, New York (1993).

[ShHo68] Shichman, H. and Hodges, D. A.: Insulated-gate field-effect transistor switching circuits. IEEE J. Solid State Circuits **SC-3**, 285–289 (1968).

[Ti99] Tischendorf, C.: Topological index calculation of differential-algebraic equations in circuit simulation. Surv. Math. Ind. **8**, 187–199 (1999).

[WCSW97] Wünsche, W., Clauß Ch., Schwarz, P., Winkler, F.: Electro-Thermal Circuit Simulation Using Simulator Coupling. IEEE Trans. VLSI Syst. **5**:3, 277–282 (1997).